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PATENT APPLICATION

ATTORNEY DOCKET NO. 10971316-1

#AF 2800

IN THE
UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): John G. McBride

Confirmation No.: 1086

Application No.: 09/311,313

Examiner: L. Garbowski

Filing Date: May 13, 1999

Group Art Unit: 2825

Title: Method and Apparatus for Determining Whether an Element in an Integrated Circuit is a Feedback Element

COMMISSIONER FOR PATENTS
Washington, D.C. 20231

TRANSMITTAL OF APPEAL BRIEF

Sir:

Transmitted herewith in **triplicate** is the Appeal Brief in this application with respect to the Notice of Appeal filed on **August 7, 2002**.

The fee for filing this Appeal Brief is (37 CFR 1.17(c)) $320.00.

(complete (a) or (b) as applicable)

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136(a) apply.

( ) (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

( )	one month	$110.00
( )	two months	$400.00
( )	three months	$920.00
( )	four months	$1440.00

( ) The extension fee has already been filled in this application.

(X) (b) Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

Please charge to Deposit Account **08-2025** the sum of **$320.00**. At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

(X) I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231. Date of Deposit: **August 15, 2002**

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Typed Name: **Hui Chin Barnhill**

Signature: H. Chin Barnhill

Respectfully submitted,

John G. McBride

By _____

Daniel R. McClure

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Date: **August 15, 2002**

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#9 Appeal Brief 8/28/02

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

In Re Application of:	)	
	)	
John G. McBride	)	Group Art Unit: 2825
	)	
Serial No.: 09/311,313	)	Examiner: Leigh Marie Garbowski
	)	
Filed: May 13, 1999	)	
	)	
For: Method And Apparatus For Determining Whether An Element In An Integrated Circuit Is A Feedback Element	)	HP Ref. 10971316-1
	)	TKHR Ref. 50814-1550
	)	

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the U.S. Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents Box: Appeal Brief, Washington, D.C. 20231 on Aug 15, 2002.

H-Ch Barnhill

Signature – Hui Chin Barnhill

APPEAL BRIEF UNDER 37 C.F.R. §1.192

Honorable Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

This is an appeal from the decision of Examiner Leigh Marie Garbowski, Group Art Unit 2825, of April 24, 2002 (Paper No. 5), rejecting claims 1-22 (although claims 2-13, 15-18, and 20-22 were indicated as having allowable subject matter) in the present application and making the rejection FINAL.

I. REAL PARTY IN INTEREST

The real party in interest of the instant application is Hewlett-Packard Company, a Delaware corporation, having its principal place of business in Palo Alto, California.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences.

III. STATUS OF THE CLAIMS

Claims 1-22 are pending in the application. The FINAL Office Action had rejected claims 1-22 under 35 U.S.C. § 112, second paragraph. However, the Advisory Action dated July 26, 2002, stated that the after-FINAL claim amendments were effective to overcome the 112 rejections. The Advisory Action, however, upheld the substantive rejections of the FINAL Office Action, which rejected claims 1, 14, and 19 under 35 U.S.C. §102(b) as being anticipated by Kuhns. The Office Action also rejected claims 1, 14, and 19 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent 6,182,268 B1, to McElvain.

IV. STATUS OF AMENDMENTS

Applicant amended independent claims 1, 14, and 19 after the FINAL Office Action. An Advisory Action mailed July 26, 2002, indicated that these claim amendments were entered. Therefore, the appendix (Tab A) of claims includes the changes made by these amendments.

V. SUMMARY OF THE INVENTION

The present invention is directed to a method and apparatus for determining (FIG. 2, reference numeral 103) whether or not an element (FIG. 4A, reference numeral 141) in an integrated circuit (138) is a feedback element (141) (specification, page 15, lines 5-13). In one embodiment, the apparatus comprises a computer capable of being configured to execute a rules checker program (100). When the rules checker program (100) is executed by the computer, it analyzes information relating to the network and determines whether or not an element (141) in the integrated circuit is a feedback element (141). In accordance with the invention, the feedback element (141) includes a transistor.

VI. CONCISE STATEMENT OF THE ISSUES PRESENTED FOR REVIEW

The issues in this appeal are: (1) whether claims 1, 14, and 19 are unpatentable under under 35 U.S.C. §102(b) as being anticipated by Kuhns. and (2) whether claims 1, 14, and 19 are unpatentable under 35 U.S.C. §102(e) as being anticipated by U.S. Patent 6,182,268 B1, to McElvain

VII. GROUPING OF THE CLAIMS

The claims of this appeal are grouped into a single claim group. The FINAL Office Action referenced claim 14 as the exemplary claim. Therefore, Applicant will address the arguments in this appeal to claim 14 as the exemplary claim of the claim group.

VIII. ARGUMENT

The FINAL Office Action rejected independent claims 1, 14, and 19 under 35 U.S.C. §102(b) as allegedly being anticipated by an article by Kuhns, entitled "Automating Testability Analysis of Analog Circuits and Systems." Applicant respectfully disagrees and requests that the Board overturn this rejection.

Taking claim 14 as the exemplary claim, claim 14 recites:

> 14. A method comprising the step of:
> ***analyzing information relating to the network to determine whether or not an element comprised in the integrated circuit is a feedback element, wherein said feedback element includes a transistor.***

(*Emphasis added.*) Claim 14 patently defines over the cited Kuhn's article because the Kuhn's article fails to disclose or otherwise teach the feature that is emphasized above.

The FINAL Office Action cited the "Testability Rules" section of the Kuhn's article (page 230) as allegedly teaching the step of determining whether or not an element of a network comprised in an integrated circuit as a feedback element (this rejection was made before Applicant amended claim 14 to recite that the feedback element included a transistor). Applicant respectfully disagrees with this rejection, and submits that the teaching and disclosure of Kuhn's falls short of properly disclosing the claimed element. In this regard, the Kuhn's article is directed to the automation of testability analysis of various analog circuits and systems. The "Testability Rules" section of the Kuhn's article, which is cited as disclosing Applicant's invention, discusses the identification of "feedback loops" within a circuit. However, and significantly, the quoted portion of Kuhn's does not disclose a method for determining whether or not an element within an integrated circuit is a feedback element. In this regard, it should be appreciated that there is a significant difference between

determining whether a given element is a feedback element, and identifying a feedback loop (which is what Kuhn's actually discloses). In this regard, Kuhn's specifically teaches:

> In the rules section, AutoTEST will search through the circuit looking for components, or configurations of components that pose unique testing problems. A prime target for this type of analysis is the identification of feedback loops. In analog circuits and systems, it is inevitable that some loops will exist. These loops can be anything from a servo control system to a simple resistive feedback circuit for an operational amplifier. It is good practice to have break points designed into most feedback loops to allow for open-loop testing. However, the smaller loops which are used within some basic circuit should not be required to be broken. Examples would be feedback to set amplifier gain or stability, simple active filters, oscillators, and simple regulators...

Simply stated, the above-quoted portion of Kuhn's does not teach, disclose, or suggest the step of determining whether or not an element in an integrated circuit is a feedback element. Furthermore, and significantly, the cited portion of the Kuhn's article is completely devoid of any teaching or suggestion that the feedback element includes a transistor. For at least this reason, claim 14 patently defines over the Kuhn's article, and the rejection based upon Kuhn's should be overturned.

The FINAL Office Action also rejected claim 14 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent 6,182,268 to McElvain. In forming this rejection, the FINAL Office Action cited column 6, lines 38-65 and column 7, lines 15-16 of McElvain as allegedly teaching the determination of whether or not an element of a network in an integrated circuit is a feedback element. Applicant respectfully disagrees. The cited portion of the McElvain states:

> In step 302, the entire circuit to be analyzed or modeled is filtered to determine which registers are likely to be part of state machine circuits. This step serves to remove extraneous circuitry such as combinational logic devices which are not coupled to registers and non-state registers (which do not have a ***feedback path*** from an output of the register back to an input to the register). In one embodiment of the present invention, the identification step 302 is performed by identifying those portions of circuitry which possess flip-flops or registers

> connected to combinational logic through one or more ***feedback paths***. A circuit consisting of a register and ***feedback path*** from the register's output to its input, such as that illustrated in FIG. 2, may usually be correctly identified as a state machine. A register which stores the current state of a state machine within a state machine is referred to as "state register." Step 302 searches through the RTL netlist description for all registers which have combinational logic in a feedback path of the register. Each register which has such logic in its ***feedback path*** is labeled as a candidate state register. Registers which do not have ***feedback paths*** (from output to input) are considered to be non-state registers. In one particular embodiment, registers in counters and arithmetic logic are considered to be non-state registers (in order to reduce analysis time for such logic which does not often benefit much from optimization). Thus, in step 302, non-state registers and those circuit elements which do not appear to be part of state machines are excluded from the circuit to be analyzed.
> ...
> a state register is defined by determining all of the devices included within the ***feedback path*** of the state register.

(*Emphasis added.*)

As can be readily verified from even a cursory reading of the cited portion of McElvain, there is absolutely no teaching nor mention of a method for determining whether a given element is a feedback element. Applicant acknowledges that McElvain appears to make broad reference to feedback paths and that registers that do not have feedback paths are considered to be non-state registers. However, it is a far stretch (to say the least) to equate the mere mention of a feedback path to the disclosure of a method for determining whether a given element within a netlist is a feedback element of an integrated circuit, as is specifically claimed in independent claim 14. Furthermore, claim 14 requires that the identified feedback element include a transistor. The McElvain reference fails to disclose this claimed feature. Accordingly, and for at least this reason, the rejection to claim 14, based upon McElvain, should be overturned by the Board.

Failure of the Advisory Action to Recognize Further Limitations of Amended Claims

The FINAL Office Action acknowledged that claims 2-13, 15-18, and 20-22 contained allowable subject matter. In commenting on the reason for allowability, paragraph 14 of the FINAL Office Action specifically stated that "the prior art of record does not specifically disclose or teach a 'field effect transistor'." In response to the FINAL Office Action, Applicant amended independent claims 1, 14, and 19 to specify that the feedback element includes a transistor. Nothing that Applicant identified in the cited art of record required Applicant to amend the claims to unduly limit the feedback element to a field effect transistor. Therefore, based upon the admission within the Office Action that the prior art of record did not disclose the feedback element as being a field effect transistor, the further limitation of the independent claims to specify that the feedback element includes a transistor is sufficient to patently define the claims over the cited art. Indeed, Applicant does not even believe that this further limitation was required, in light of the failed teachings of the cited art.

Not withstanding this amendment to the claims, however, the Advisory Action, which was mailed July 26, 2002, merely stated that the amendments did not place the application in condition for allowance because "the proposed amendments do not include all of the features recited in the objected claims."

This reflects a fundamental error on the part of the Office Action. Specifically, the independent claims need not be amended to include all of the limitations of the dependent claims. Rather, the independent claims need be amended only to the extent necessary to define over the cited art. Again, it is Applicant's position that no amendment was necessary. However, to accommodate the admissions of the Office Action, Applicant amended the independent claims to specify that the feedback element included a transistor. Based upon

the admissions of the Office Action, in view of the teachings of the cited references, the amendment should have been sufficient to clearly place the independent claims in condition for allowance. Failure of the Office Action (i.e., the Advisory Action) to recognize this patentably-defining feature, reflects an error on the part of the Office Action, which should be overturned by the Board.

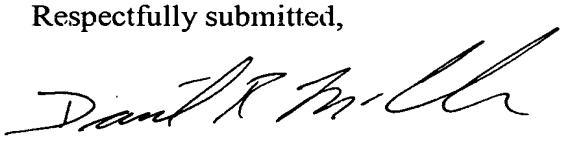
For at least the foregoing reasons, Applicant respectfully requests that the Board overturn the rejections of claim 14 (as well as claims 1 and 19) based upon both the Kuhn's article and the McElvain patent.

IX. CONCLUSION

Based upon the foregoing discussion, Applicants respectfully requests that the Examiner's FINAL rejection of claims 1-22 be overturned by the Board, and that the application be allowed to issue as a patent with all pending claims 1-22.

Please charge Hewlett-Packard Company's deposit account 08-2025 in the amount of $310 for the filing of this Appeal Brief. No additional fees are believed to be due in connection with this Appeal Brief. If, however, any additional fees are deemed to be payable, you are hereby authorized to charge any such fees to deposit account No. 08-2025.

Respectfully submitted,



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X. APPENDIX

Claims

1. An apparatus comprising:

logic configured to analyze information relating to the network to determine whether or not an element comprised in the integrated circuit is a feedback element, wherein said feedback element includes a transistor.

2. The apparatus of claim 1, wherein said logic is a computer configured to execute a rules checker program, wherein when the rules checker program is run on the computer, the rules checker program analyzes the information relating to the network to determine whether or not the element is a feedback element, wherein the element is a field effect transistor.

3. The apparatus of claim 2, wherein the rules checker program first determines whether or not the element being evaluated is a comprised in a recycle loop, wherein if a determination is made that the element is not comprised in a recycle loop, the rules checker program determines that the element is not a feedback element.

4. The apparatus of claim 3, wherein if the rules checker program determines that the transistor is comprised in a recycle loop, then the rules checker program determines whether or not a source or drain terminal of the transistor is connected to a RAM cell; wherein if the rules checker program determines that the source or drain of the transistor is connected to a RAM cell, the rules checker program determines that the transistor is a feedback element.

5. The apparatus of claim 4, wherein if the rules checker program determines that source or drain of the transistor is not connected to a RAM cell, the rules checker program determines whether or not a gate terminal of the transistor being evaluated is a precharge node, wherein if the rules checker program determines that the gate terminal of the transistor is a precharge node, the rules checker program determines that the transistor is not a feedback element.

6. The apparatus of claim 5, wherein if the rules checker program determines that the gate terminal of the transistor is not a precharge node, the rules checker program determines whether or not the gate terminal of the transistor corresponds to a block input of the network comprising the transistor, wherein if the rules checker program determines that the gate terminal of the transistor being evaluated is a block input, the rules checker program determines that the transistor being evaluated is not a feedback element.

7. The apparatus of claim 6, wherein if the rules checker program determines that the gate terminal of the transistor being evaluated is not a block input, then the rules checker program determines whether or not an output of a return inverter comprised by the recycle loop is only driven by the return inverter, wherein if the rules checker program determines that the output of the return inverter is only driven by the return inverter, the rules checker program determines that the transistor being evaluated is not a feedback element.

8. The apparatus of claim 7, wherein if the rules checker determines that the output of the return inverter is not driven only by the return inverter, the rules checker program determines whether or not a gate terminal of the transistor being evaluated is driven by a pass transistor, wherein if the rules checker program determines that the gate terminal of the transistor is driven by a pass transistor, the rules checker program determines that the

transistor being evaluated is not a feedback element, wherein if the rules checker program determines that the gate terminal of the transistor being evaluated is not driven by a pass transistor, the rules checker program determines whether or not the gate terminal is channel-connected to another transistor which is not controlled either by a clock or by an output of the logic gate comprising the transistor being evaluated, wherein if the rules checker program determines that the gate terminal is not channel-connected to another transistor which not is controlled by a clock or by an output of the logic gate comprising the transistor being evaluated, the rules checker program determines that the transistor being evaluated is a feedback element.

9. The apparatus of claim 8, wherein the recycle loop comprises a first inverter and a second inverter, the transistor being evaluated being comprised in the first inverter, the first inverter corresponding to said logic gate, wherein if the rules checker program determines that the gate terminal is channel-connected to another transistor which is not controlled either by a clock or by an output of the logic gate comprising the transistor being evaluated, the rules checker program determines whether an N field effect transistor network and a P field effect transistor network comprised in the first inverter are both stronger than an N field effect transistor network and a P field effect transistor network, respectively, comprised in the second inverter, wherein if the rules checker program determines that the N field effect transistor network and the P field effect transistor network comprised in the first inverter are both stronger than the N field effect transistor network and the P field effect transistor network comprised in the second inverter, the rules checker program determines that the transistor being evaluated is not a feedback element.

10. The apparatus of claim 9, wherein if the rules checker program determines that

the N field effect transistor network and the P field effect transistor network comprised in the first inverter are both stronger than the N field effect transistor network and the P field effect transistor network comprised in the second inverter, the rules checker program determines whether an N field effect transistor network and a P field effect transistor network comprised in the first inverter are both weaker than the N field effect transistor network and the P field effect transistor network, respectively, comprised in the second inverter, wherein if the rules checker program determines that the N field effect transistor network and the P field effect transistor network comprised in the first inverter are not both weaker than the N field effect transistor network and the P field effect transistor network comprised in the second inverter, the rules checker program determines that the transistor being evaluated is a feedback element.

11. The apparatus of claim 2, wherein the rules checker program determines whether or not the transistor being evaluated is a feedback element by determining whether or not the transistor is comprised in a particular type of circuit, the particular type of circuit corresponding to a special case, wherein if the rules checker program determines that the element being evaluated is comprised in the particular type of circuit, the rules checker program determines that the transistor being evaluated is a feedback element.

12. The apparatus of claim 11, wherein the particular type of circuit corresponds to a zero catcher circuit and wherein the rules checker program performs a plurality of checks to determine whether or not the particular type of circuit is a zero catcher circuit.

13. The apparatus of claim 12, wherein the particular type of circuit corresponds to a ones catcher circuit and wherein the rules checker program performs a plurality of checks to determine whether or not the particular type of circuit is a ones catcher circuit.

14. A method comprising the step of:

analyzing information relating to the network to determine whether or not an element comprised in the integrated circuit is a feedback element, wherein said feedback element includes a transistor.

15. The method of claim 14, wherein the analyzing step is performed by a computer configured to perform the analysis, wherein said computer is configured to execute a rules checker program, wherein when the rules checker program runs on the computer, the rules checker program analyzes the information relating to the network to determine whether or not the element is a feedback element, wherein the element is a field effect transistor.

16. The method of claim 15, wherein during the analyzing step, the rules checker program first determines whether or not the element being evaluated is comprised in a recycle loop, wherein if a determination is made that the transistor is not comprised in a recycle loop, the rules checker program determines that the transistor is not a feedback element.

17. The method of claim 16, wherein if, during the analyzing step, the rules checker program determines that the transistor is comprised by a recycle loop, then the rules checker program determines whether or not a source or drain of the transistor is connected to a RAM cell, wherein if the rules checker program determines that the source or drain of the transistor is connected to a RAM cell, the rules checker program determines that the transistor is a feedback element.

18. The method of claim 17, wherein if, during the analyzing step, the rules checker program determines that the source or drain of the transistor is not part of a RAM

cell, then the rules checker program determines whether or not a gate terminal of the transistor being evaluated is a precharge node, wherein if the rules checker program determines that the gate terminal of the transistor being evaluated is a precharge node, the rules checker program determines that the transistor being evaluated is not a feedback element.

19. A computer program comprising:

a first code segment which analyzes information relating to the network to determine whether or not an element comprised in the integrated circuit is a feedback element, wherein said feedback element includes a transistor.

20. The computer program of claim 19, wherein the first code segment first determines whether or not the element being evaluated is comprised in a recycle loop, wherein if a determination is made by the first code segment that the transistor is not comprised in a recycle loop, the program determines that the transistor is not a feedback element.

21. The program of claim 20, wherein if the first code segment determines that the transistor is comprised by a recycle loop, then the first code segment determines whether or not a source or drain of the transistor is connected to a RAM cell, wherein if the first code segment determines that the source or drain of the transistor is connected to a RAM cell, the program determines that the transistor is a feedback element, and wherein if first code segment determines that the source or drain of the transistor is not part of a RAM cell, then the first code segment determines whether or not the gate terminal of the transistor is a precharge node, wherein if the rules checker program determines that the gate terminal of the

transistor is a precharge node, the rules checker program determines that the transistor is not a feedback element.

22. The computer program of claim 19, wherein the first code segment determines whether or not the element being evaluated is a feedback element by determining whether or not the element is comprised in a particular type of circuit, the particular type of circuit corresponding to a special case, wherein if the first code segment determines that the element being evaluated is comprised in the particular type of circuit, the first code segment determines that the element being evaluated is a feedback element.